User manual PCI/
Serial Highway Controller

BLN 99-13 UM

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IMPORTANT NOTICE

SWITCH OFF THE SYSTEM POWER BEFORE INSTALLING OR REMOVING THIS INTERFACE.

IGNORING THIS ADVICE MAY RESULT IN PERMANENT DAMAGE TO THIS INTERFACE OR TO OTHER INTERFACES.

Table of contents page

1. Introduction 5

2. Block diagram of the PCI/Serial Highway Controller 7

3. PCI/Serial Highway Controller global programming model 9

4. Programming model of the PCI configuration space 11
   - 4.1 Vendor ID register 12
   - 4.2 Device ID register 12
   - 4.3 Command register 12
   - 4.4 Status register 14
   - 4.5 Revision ID register 16
   - 4.6 Class code register 16
   - 4.7 PCI Base Address Register 0 for memory-mapped Configuration Registers (PCIBAR0) 17
   - 4.8 PCI Base Address Register 2 for Local Address Space 0 (PCIBAR2) 18
   - 4.9 Subsystem Vendor ID register 19
   - 4.10 Subsystem ID register 19
   - 4.11 Interrupt Line register 19
   - 4.12 Interrupt Pin register 19
   - 4.13 Unimplemented or unused PCI Configuration Space registers 20

5. Programming model of the PCI 9080 I/O Accelerator interface chip 21
   - 5.1 Local Configuration Registers 22
     - 5.1.1 Range for PCI-to-Local Address Space 0 24
     - 5.1.2 Local Base Address (Remap) for PCI-to-Local Address Space 0 . . . 25
     - 5.1.3 Mode/Arbitration Register 25
     - 5.1.4 Big/Little Endian Descriptor Register 28
     - 5.1.5 Local Bus Region Descriptors (Space 0 and Expansion ROM) for PCI-to-Local Accesses 29
   - 5.2 Runtime Registers 32
     - 5.2.1 Interrupt Control / Status Register 33
     - 5.2.2 Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register 36
     - 5.2.3 Vendor ID 37
     - 5.2.4 Device ID 37
     - 5.2.5 Revision ID 37

5.3 DMA Registers 38
5.3.1 DMA Channel 0 Mode Register 39
5.3.2 DMA Channel 0 PCI Address Register 41
5.3.3 DMA Channel 0 Local Address Register 41
5.3.4 DMA Channel 0 Transfer Byte Count Register 41
5.3.5 DMA Channel 0 Descriptor Pointer Register 42
5.3.6 DMA Channel 0 Command/Status Register 43
5.3.7 DMA Mode/Arbritration Register 43
5.3.8 DMA Threshold Register 44

6. Programming model of the Serial Highway control section 45
6.1 Control and Status Register 46
6.2 PhyBUS (DMA) Address Register 49
6.3 PhyBUS Word Data Register 49
6.4 Interrupt Enquiry Register 50
6.5 PhyBUS Long Word Data Register 50
6.6 Maintenance Control and Status Register 51
6.7 Maintenance Word Data Register 52
6.8 Maintenance Long Word Data Register 52
6.9 Protocol Error Register Slave 53
6.10 Protocol Error Register Master 55
6.11 Interrupt Control and Status Register 56
6.12 Bus Error Address Register 58
6.13 Swap Select Register 59
6.14 EPLD Configuration Register 60

7. Description of the maintenance modes 63
7.1 Maintenance mode 0 63
7.2 Maintenance mode 1 63
7.3 Maintenance mode 2 64

Appendix A. Serial EEPROM initialisation data 65

1. Introduction

The PCI/Serial Highway Controller is a PCI compliant device used for interfacing the TueDACS data acquisition system to the industry-standard PCI Bus. A complete TUeDACS system configuration consists of 3 parts:

- the PCI/Serial Highway Controller located in the PCI bus (BLN 99-15);
- - the Serial Highway/TUeDACS Controller (SHP, BLN 98-18) located in a TUeDACS system crate, or
  - a TUeDACS/1 module;
- the interconnecting cable

The main features of the PCI/Serial Highway Controller are:

- PCI interface is based on the industry standard PLX PCI 9080 I/O Accelerator interface chip
- PCI revision 2.1 compliant
- full TUeDACS bus signal support
- 32-bit and 16-bit TUeDACS bus access
- 32-bit and 16-bit DMA facilities
- TUeDACS interrupt support
- 4 modes of byte lane swapping to support both big-endian and little-endian processor architectures

2. Block diagram of the PCI/Serial Highway Controller

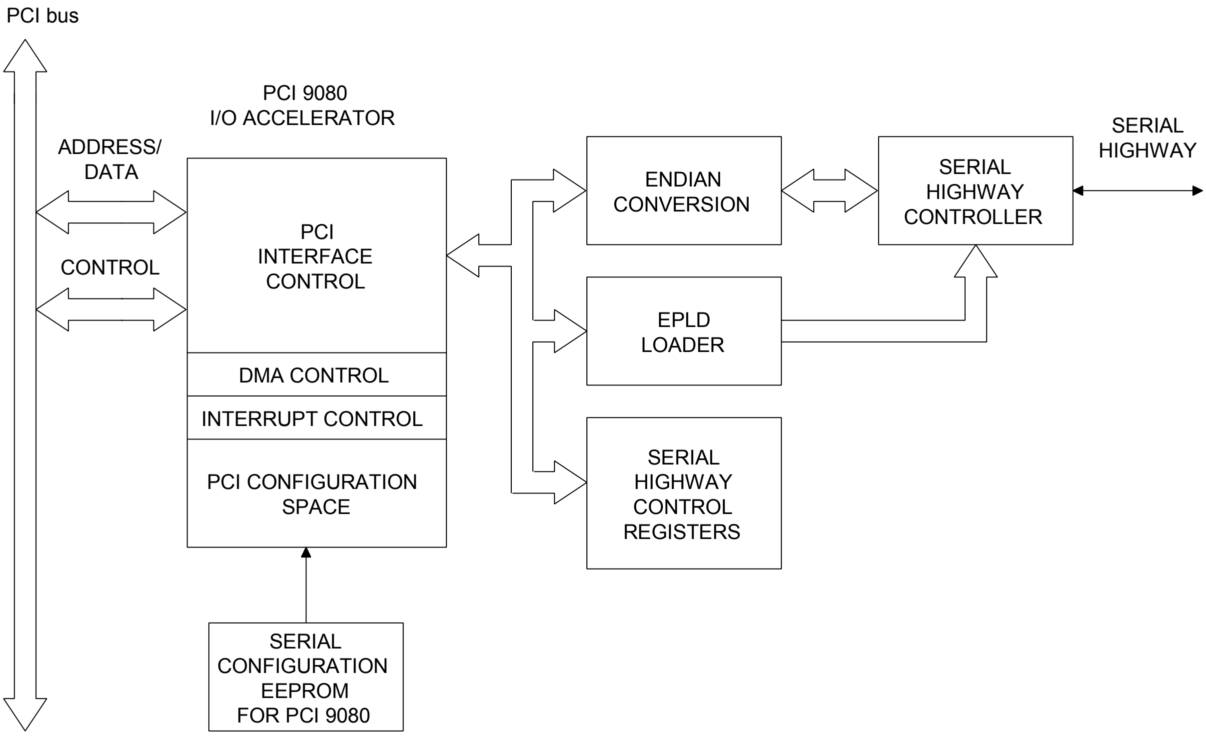

Figure 2.1 Block diagram of the PCI/Serial Highway Controller

3. PCI/Serial Highway Controller global programming model

The PCI/Serial Highway Controller global programming model consists of 3 sections:

- programming model of the PCI configuration space (section 4)
- programming model of the PCI 9080 I/O Accelerator interface chip (section 5)
- programming model of the Serial Highway Control section (section 6)

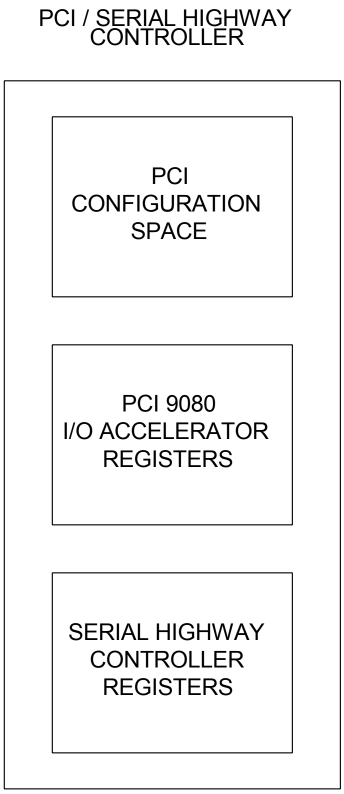

Figure 3.1 PCI/Serial Highway Controller global programming model

4. Programming model of the PCI configuration space

The programming model of the PCI configuration space complies with the programming model as defined by the PCI Local Bus specification. The PCI configuration space is loacted in the PCI 9080 I/O Accelerator chip. On the PCI/Serial Highway Controller, only the 64-byte header of the 256-byte configuration space is implemented, see figure 4.1.

For a detailed description of functions in the configuration space, see the PCI Local Bus specification.

<table>
<tr><th colspan="2">31 … 16</th><th colspan="2">15 … 0</th><th></th></tr>
<tr><td colspan="2">DEVICE ID</td><td colspan="2">VENDOR ID</td><td>0x00</td></tr>
<tr><td colspan="2">STATUS</td><td colspan="2">COMMAND</td><td>0x04</td></tr>
<tr><td colspan="3">CLASS CODE</td><td>REVISION ID</td><td>0x08</td></tr>
<tr><td>BIST</td><td>HEADER TYPE</td><td>LATENCY TIMER</td><td>CACHE LINE SIZE</td><td>0x0C</td></tr>
<tr><td colspan="4">PCI BASE ADDRESS 0 FOR MEMORY-MAPPED CONFIGURATION REGISTERS (PCIBAR0)</td><td>0x10</td></tr>
<tr><td colspan="4">PCI BASE ADDRESS 1 FOR I/O-MAPPED CONFIGURATION REGISTERS (PCIBAR1)</td><td>0x14</td></tr>
<tr><td colspan="4">PCI BASE ADDRESS 2 FOR LOCAL ADDRESS SPACE 0 (PCIBAR2)</td><td>0x18</td></tr>
<tr><td colspan="4">PCI BASE ADDRESS 2 FOR LOCAL ADDRESS SPACE 1 (PCIBAR3)</td><td>0x1C</td></tr>
<tr><td colspan="4">UNUSED BASE ADDRESS (PCIBAR4)</td><td>0x20</td></tr>
<tr><td colspan="4">UNUSED BASE ADDRESS (PCIBAR5)</td><td>0x24</td></tr>
<tr><td colspan="4">CARDBUS CIS POINTER (NOT SUPPORTED)</td><td>0x28</td></tr>
<tr><td colspan="2">SUBSYSTEM ID</td><td colspan="2">SUBSYSTEM VENDOR ID</td><td>0x2C</td></tr>
<tr><td colspan="4">PCI BASE ADDRESS FOR LOCAL EXPANSION ROM</td><td>0x30</td></tr>
<tr><td colspan="4">RESERVED</td><td>0x34</td></tr>
<tr><td colspan="4">RESERVED</td><td>0x38</td></tr>
<tr><td>MAX_LAT</td><td>MIN_GNT</td><td>INTERRUPT PIN</td><td>INTERRUPT LINE</td><td>0x3C</td></tr>
</table>

Figure 4.1 PCI configuration space

4.1 Vendor ID register

This 16-bit read-only register at subaddress 0x00 is loaded from the serial configuration EEPROM. If a programmed EEPROM is present, this register holds the value 0xfffe, representing the vendor id of the TU/e Physical and Technical Laboratory Automation Group. If the EEPROM is not present, or the EEPROM is blank, this register holds a default value of 0x10b5, representing the PLX vendor id.

4.2 Device ID register

This 16-bit read-only register at subaddress 0x02 is loaded from the serial configuration EEPROM. If a programmed EEPROM is present, this register holds the value 0x0002, representing the device id of the PCI/Serial Highway Controller. If the EEPROM is not present, or the EEPROM is blank, this register has a default value of 0x9080, representing the PLX part number of the PCI 9080 interface chip.

4.3 Command register

This 16-bit read/write register at subaddress 0x04 provides coarse control to generate and respond to PCI cycles. If the value 0x00 is written to this register, the PCI/Serial Highway Controller is logically disconnected from the PCI bus for all accesses except configuration space accesses. After a system reset, this register holds the value 0x00.

X	X	X	X	X	X	FBBE	SERE	X	PER	X	MWI	X	ME	MS	IOS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 4.2 Command register

bit	mnemonic	R/W	description
15..10	-	-	not used, read as zero
9	FBBE	RO	Fast Back-to-Back Enable
8	SERE	R/W	SERR# Enable
7	-	-	not used, reads as zero
6	PER	R/W	Parity Error Response
5	-	-	not used, reads as zero
4	MWI	R/W	Memory Write and Invalidate
3	-	-	not used, reads as zero
2	ME	R/W	Master Enable
1	MS	R/W	Memory Space
0	IOS	R/W	I/O Space

FBBE (bit 9): Fast Back-to-Back Enable. This bit must be set to zero.

SERE (bit 8): SERR# Enable. This bit must be set to zero.

PER (bit 6): Parity Error Response. Setting this bit enables parity error detection, clearing this disables parity error detection.

MWI (bit 4): Memory Write and Invalidate. This bit must be set to zero.

ME (bit 2): Master Enable. Setting this bit allows the PCI/Serial Highway Controller to behave as a PCI bus master. Clearing this bit disables the controller to behave as a PCI bus master. The ME bit must be set before executing a DMA operation.

MS (bit 1): Memory Space. Setting this bit allows the PCI/Serial Highway Controller to respond to Memory Space accesses. Clearing this bit disables the controllers response to Memory Space accesses, i.e. no PCI 9080 I/O interface registers, nor Serial Highway Controller registers (see section 6) can be accessed.

IOS (bit 0): IO Space. Setting this bit allows the PCI/Serial Highway Controller to respond to IO Space accesses. As no IO space accesses are needed, this bit must be set to 0.

4.4 Status register

This 16-bit read/write register at subaddress 0x06 is used for recording status information for PCI bus related events.

Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is cleared whenever the register is written, and the corresponding data bit is set.

DPE	SSE	MA	RTA	TA	DT1	DT0	DPD	FBBC	UDF	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 4.3 Status register

bit	mnemonic	R/W	description
15	DPE	R/W	Detected Parity Error
14	SSE	R/W	Signaled System Error
13	MA	R/W	Master Abort
12	RTA	R/W	Received Target Abort
11	TA	R/W	Target Abort
10	DT1	RO	DEVSEL timing, bit 1
9	DT0	RO	DEVSEL timing, bit 0
8	DPD	RO	Data Parity Detected
7	FBBC	RO	Fast Back-to-Back Capable
6	UDF	RO	User Definable Features supported
5..0	-	-	reserved, always read as zero

DPE (bit 15): Detected Parity Error. When set to 1, indicates that the PCI 9080 has detected a PCI bus parity error, even if parity error handling is disabled. (PER bit in the command register is cleared). This bit is set if:

- the PCI 9080 detected a parity error during the PCI address phase, or
- the PCI 9080 detected a data parity error when it was a target of write, or
- the PCI 9080 detected a data parity error when performing a Master Read operation.

Writing a 1 to the DPE bit clears this bit.

SSE (bit 14): Signaled System Error. When set to 1, indicates that the PCI 9080 has reported a system error on the SERR# signal. Writing a 1 to the SSE bit clears this bit.

MA (bit 13): Master Abort. This bit is set by the PCI/Serial Highway Controller if the controller is PCI bus master and when a transaction is terminated with Master-Abort, i.e. a DMA transaction is in progress, and a TUeDACS bus or a PCI-bus bus error occurs. Writing a 1 to the MA bit clears this bit. This bit is not used on the PCI/Serial Highway Controller.

RTA (bit 12): Received Target Abort. This bit is set by the PCI/Serial Highway Controller if a DMA transaction is terminated with Target-Abort, i.e. a device on the PCI-bus asserts the STOP# signal line and deasserts DEVSEL# on the same clock. This bit can only be set if the controller is bus master (i.e. if the controller is programmed for DMA operation). Writing a 1 to the RTA bit clears this bit.

TA (bit 11): Signaled Target Abort. This bit is set by the PCI/Serial Highway Controller if the controller is a PCI target, i.e. the controller is not programmed for DMA operation, and if a transaction is terminated with Target-Abort, i.e. a TUeDACS bus error occurs. Writing a 1 to the TA bit clears this bit. This bit is not used on the PCI/Serial Highway Controller.

DT1..DT0 (bits 10..9): DEVSEL Timing. These bits are hardcoded to 01 (medium DEVSEL timing).

DPD (bit 8): Data Parity Detected. This bit is set if the following 3 conditions are met:

- ❑ the PCI 9080 asserted PERR# itself or observed PERR# asserted, and
- ❑ the PCI 9080 was bus master for the operation in which the error occurred, and
- ❑ the PER bit in the Command register is set.

Writing a 1 to the bit clears this bit.

FBBC (bit 7): Fast Back-to-Back capable. If this bit is set, it indicates that the controller can accept fast back-to-back transactions. If this bit is cleared, no fast back-to-back transactions can be accepted. This bit is always set to 1.

UDF (bit 6): User Definable Features supported. If this bit is set, user definable features are supported. If this bit is cleared, user definable features are not supported. This bit is always set to 1.

4.5 Revision ID register

This 8-bit read-only register at subaddress 0x08 is loaded from the serial configuration EEPROM. If a programmed EEPROM is present, this register identifies the revision level of the PCI/Serial Highway Controller. If the EEPROM is not present, or the EEPROM is blank, this register holds the revision level of the PCI 9080 interface chip.

4.6 Class code register

This 24-bit read-only register at subaddress 0x09 is loaded from the serial configuration EEPROM. If a programmed EEPROM is present, this register holds the value 0x068000: base class = 0x06 (PCI/Serial Highway Controller is a bridge device), subclass = 0x80, interface = 0x00. If the EEPROM is not present, or the EEPROM is blank, the Class code register holds a default value of 0x068000: base class = 0x06 (bridge device), subclass = 0x80 (other bridge device) , interface = 0x00.

4.7 PCI Base Address Register 0 for memory-mapped Configuration Registers (PCIBAR0)

This 32-bit read/write register at subaddress 0x10 must be initialized by a POST-routine (Power-On Self Test) during system boot. After initialization, this register holds the physical memory base address in system memory space of the internal Configuration Registers (256 byte locations containing the Local, Runtime and DMA Registers in the subaddress range 0x00..0xff) of the PCI 9080 interface chip.

To obtain the memory space required by the internal Configuration Registers, the POST routine must take the following steps:

- ❑ write a value of all 1's (0xffffffff) to this register
- ❑ read the register
- ❑ determine the memory space required
- ❑ write the base address of this memory space into this register

The bits 31..8 read as 1 after writing all 1's to Base Address Register 0. The bits 7..4 always read as zero (harcoded in the PCI 9080 interface chip). The number of consecutive zero-bits in bit positions 31..4 (starting at bit 4) define the number of 16-byte chunks the internal Configuration Registers occupy in system memory space. As there are 4 0-bits (bit 7..4), the Configuration Registers occupy $2^4 * 16$ bytes = 256 bytes of system memory space. See also the programming model of the PCI 9080 interface chip (section 5).

According to the PCI Local Bus specification, the following description applies to bits 3..0 of PCI Base Address Register 0 (these 4 bits are hardcoded to 0 in the PCI 9080 interface chip):

bit 3:	reads as zero, prefetching is not used
bits 2..1:	read as zero, the PCI 9080 Configuration Registers can be located anywhere in the 32-bit memory address space.
bit 0:	reads as zero, the PCI 9080 Configuration Registers map into memory space.

User software does not need to initialize the PCIBAR0 register, as the POST routine already takes care of mapping the PCI 9080 interface chip into the available system memory space. Changing the contents of PCIBAR0 may result in erroneous operation.

4.8 PCI Base Address Register 2 for Local Address Space 0 (PCIBAR2)

This 32-bit read/write register at subaddress 0x18 must be initialized by a POST-routine (Power-On Self Test) during system boot. After initialization, this register holds the physical memory base address in system memory space of the Serial Highway Controller registers (64 byte locations, subaddress range 0x00..0x3c).

To obtain the memory space required by the Serial Highway Controller registers, the POST routine must take the following steps:

- ❑ write a value of all 1's (0xffffffff) to this register
- ❑ read the register
- ❑ determine the memory space required
- ❑ write the base address of this memory space into this register

The bits 31..6 read as 1 after writing all 1's to PCI Base Address Register 2. The bits 5..4 read as zero. The number of consecutive zero-bits in bit positions 31..4 (starting at bit 4) define the number of 16-byte chunks the Serial Highway Controller registers occupy in system memory space. As there are two 0-bits (bits 5..4), these registers occupy $2^2 * 16$ bytes = 64 bytes of system memory space. See also the programming model of the Serial Highway Controller (section 6).

According to the PCI Local Bus specification, the following description applies to bits 3..0 of PCI Base Address Register 2 (these 4 bits are loaded from the serial configuration EEPROM when a reset occurs):

bit 3:	reads as zero, prefetching is not used
bits 2..1:	read as zero, the Serial Highway Controller registers can be located anywhere in the 32-bit memory address space.
bit 0:	reads as zero, the Serial Highway Controller registers map into memory space.

The value read from PCIBAR2 is determined by the contents of the Local Address Space 0 Range Register (LAS0RR) at memory address PCIBAR0 + 0x00. The LAS0RR register is loaded from the serial configuration EEPROM when a reset occurs.

User software does not need to initialize the PCIBAR2 register, as the POST routine already takes care of mapping the Serial Highway Controller registers into the available system memory space. Changing the contents of PCIBAR2 may result in erroneous operation.

4.9 Subsystem Vendor ID register

This 16-bit read-only register at subaddress 0x2c is loaded from the serial configuration EEPROM. If a programmed EEPROM is present, this register identifies the current revision level of the PCI/Serial Highway Controller. If the EEPROM is not present, or the EEPROM is blank, this register has a default value of 0x10b5, representing the PLX vendor id.

4.10 Subsystem ID register

This 16-bit read-only register at subaddress 0x2e is loaded from the serial configuration EEPROM. The value contained in this 16-bit read-only register at subaddress 0x2e depends on the form factor of the PCI/Highway controller. Currently, the only available form factor is for the PC. If a programmed EEPROM is present, this register has a value of 0x9913. If the EEPROM is not present, or the EEPROM is blank, this register has a value of 0x9080, representing the PLX part number of the PCI 9080 interface chip.

4.11 Interrupt Line register

This 8-bit read/write register at subaddress 0x3c is used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The PCI/Serial Highway Controller does not use this value, rather it can be used by a device driver to determine priority and vector information.

The value in this register is system architecture specific. For x86 based PC's, the values in this register correspond to IRQ numbers (0..15) of the standard dual 8259 configuration. The value 255 is defined as meaning 'unknown' or 'no connection' to the interrupt controller. Values between 15 and 255 are reserved.

The Interrupt Line register is initialized by POST (Power-On Self Test) software.

4.12 Interrupt Pin register

This 8-bit read-only register at subaddress 0x3d is used to identify the interrupt pin on the PCI-bus of the PCI/Serial Highway Controller. As the PCI 9080 interface chip only supports INTA#, the Interrupt Pin register always reads as 0x01.

This register is loaded from the serial configuration EEPROM. After loading, this register has a fixed value of 0x01. After a system reset, this register also has a value of 0x01.

4.13 Unimplemented or unused PCI Configuration Space registers

The following PCI Configuration Space registers are unimplemented or unused on the PCI/Serial Highway Controller:

	subaddress	register
❑	0x0c	BIST register
❑	0x0d	Header Type register
❑	0x0e	PCI Latency Timer register
❑	0x0f	Cache Line Size register
❑	0x14	PCI Base Address Register 1
❑	0x1c	PCI Base Address Register 3
❑	0x20	PCI Base Address Register 4
❑	0x24	PCI Base Address Register 5
❑	0x28	Cardbus CIS pointer
❑	0x30	Expansion ROM Base Address register
❑	0x3c	Max_Lat register
❑	0x3d	Min_Gnt register

5. Programming model of the PCI 9080 I/O Accelerator interface chip

The programming model of the PCI 9080 I/O Accelerator interface chip consists of 3 sections, see figure 5.1:

- ❑ Local Configuration Registers (0x00..0x2c, 0xf0..0xf8)
- ❑ Runtime Registers (0x40..0x7c)
- ❑ DMA Registers (0x08..0xb0)

All subaddresses in this programming model are relative to the base address contained in PCI Base Address Register 0 for Memory Mapped Configuration Registers (PCIBAR0). PCIBAR0 is located at subaddress 0x10 in the the PCI configuration space, see section 4. The PCIBAR0 register holds the physical memory start address in system memory space of these registers.

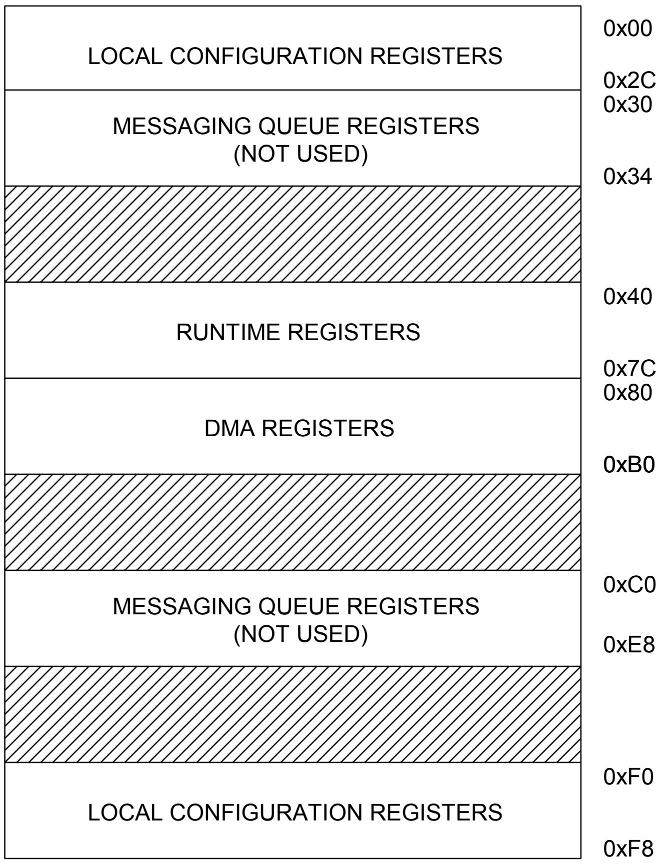

Figure 5.1 Programming model of the PCI 9080 I/O Accelerator interface chip

5.1 Local Configuration Registers

The programming model of the Local Configuration Registers is given in figure 5.2.

RANGE FOR PCI-TO-LOCAL ADDRESS SPACE 0	0x00
LOCAL BASE ADDRESS (REMAP) FOR PCI-TO-LOCAL ADDRESS SPACE 0	0x04
MODE/ARBITRATION REGISTER	0x08
BIG/LITTLE ENDIAN DESCRIPTOR REGISTER	0x0C
RANGE FOR PCI-TO-LOCAL EXPANSION ROM	0x10
LOCAL BASE ADDRESS (REMAP) FOR PCI-TO-LOCAL EXPANSION ROM AND BREQ0 CONTROL	0x14
LOCAL BUS REGION DESCRIPTORS (SPACE 0 AND EXPANSION ROM) FOR PCI-TO-LOCAL ACCESSES	0x18
RANGE FOR DIRECT MASTER TO PCI	0x1C
LOCAL BASE ADDRESS FOR DIRECT MASTER TO PCI MEMORY	0x20
LOCAL BASE ADDRESS FOR DIRECT MASTER TO PCI I/O CFG	0x24
PCI BASE ADDRESS (REMAP) FOR DIRECT MASTER TO PCI	0x28
PCI CONFIGURATION ADDRESS REGISTER FOR DIRECT MASTER TO PCI I/O CFG	0x2C
RANGE FOR PCI-TO-LOCAL ADDRESS SPACE 1	0xF0
LOCAL BASE ADDRESS (REMAP) FOR PCI-TO-LOCAL ADDRESS SPACE 1	0xF4
LOCAL BUS REGION DESCRIPTOR (SPACE 1) FOR PCI-TO-LOCAL ACCESS	0xF8

Figure 5.2 Local Configuration Register programming model

The following Local Configuration Registers are unused on the PCI/Serial Highway Controller:

	subaddress	register
❑	0x10	Range for PCI-to-Local Expansion ROM
❑	0x14	Local Base Address (Remap) for PCI-to-Local Expansion ROM and BREQ0 Control
❑	0x1c	Range for Direct Master to PCI
❑	0x20	Local Base Address for Direct Master to PCI Memory
❑	0x24	Local Base Address for Direct Master to PCI IO/CFG
❑	0x28	PCI Base Address (Remap) for Direct Master to PCI
❑	0x2c	PCI Configuration Address Register for Direct Master to PCI IO/CFG
❑	0xf0	Range for PCI-to-Local Address Space 1
❑	0xf4	Local Base Address (Remap) for PCI-to-Local Address Space 1
❑	0xf8	Local Bus Region Descriptor (Space 1) for PCI-to-Local Accesses

5.1.1 Range for PCI-to-Local Address Space 0

This 32-bit read/write register at subaddress 0x00 maps the PCI memory address range of the registers in the Serial Highway control section in Local Address Space 0, see section 6. This register is loaded from EEPROM, if a programmed EEPROM is present. This register has the following bits:

bits 31..4: specifies which PCI address bits to use for decoding PCI accesses to Local Bus Space 0. Each bit corresponds to a PCI address bit. Bit 31 corresponds to address bit 31. Write a 1 to all bits to be included in decode and a 0 to all others. These bits are used in conjunction with PCI Base Address Register 2 for Local Address Space 0 (PCIBAR2) at subaddress 0x18 in PCI configuration space.
BLN 99-13: as the Serial Highway Control section on the PCI/Serial Highway Controller occupies 64 bytes of system memory space, address bits 6..0 need *not* to be decoded. This implies that bits 31..7 must be set to 1, and bits 6..4 must be set to 0.

bit 3: if mapped into memory space, a value of 1 indicates reads are prefetchable. If mapped into I/O space, bit 3 is included with bits 31..2 to indicate decoding range.
BLN 99-13: the local bus is mapped into memory space: bit 3 must be set to 0 (reads are not prefetchable).

bits 2..1: if mapped into memory space, encoding is as follows:

bit 2	bit 1	meaning
0	0	locate anywhere in 32-bit PCI address space
0	1	locate below 1 MB in PCI address space
1	0	locate anywhere in 64-bit PCI address space
1	1	reserved

If mapped into I/O space, bit 1 must be set to 0 and bit 2 is included with bits 31..3 to indicate decoding range.
BLN 99-13: the local bus is mapped into 32-bit PCI memory space: bits 2..1 must both be set to 0.

bit 0: Memory Space Indicator. A value of 0 indicates Local Address Space 0 maps into PCI memory space. A value of 1 indicates Local Address Space 0 maps into PCI I/O space.
BLN 99-13: the Local Address Space 0 is mapped into 32-bit PCI memory space: bit 0 must be set to zero.

5.1.2 Local Base Address (Remap) for PCI-to-Local Address Space 0

This register is loaded from EEPROM, if a programmed EEPROM is present. This 32-bit read/write register at subaddress 0x04 has the following bits:

bits 31..4: remap of PCI address to Local Address Space 0 into a Local Address Space. Remap (replace) PCI address bits used in decode as Local Address bits.
BLN 99-13: no replacing used: bits 31..4 must be set to 0.

bits 3..2: if Local Address Space 0 is mapped into memory space, bits are not used. If Local Space 0 is mapped into I/O space, bits are included with bits 31..4 for remapping.
BLN 99-13: Local Address Space 0 is mapped into memory space: bits 3..2 are not used and must be set to 0.

bit 1: reserved, always reads as 0

bit 0: Local Address Space 0 Enable. A value of 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 0. A value of 0 disables decoding. If set to 0, PCI BIOS may not allocate a base address for Local Address Space 0. This bit must be set to 1 for any Direct Slave access to Local Address Space 0.
BLN 99-13: Local Address Space must be accessible: bit 0 must be set to 1.

5.1.3 Mode/Arbitration Register

This register is loaded from EEPROM, if a programmed EEPROM is present. This 32-bit read/write register at subaddress 0x08 has the following bits:

bits 31..30: reserved, always read as zero

bit 29: if this bit is set to 0, reading subaddress 0x00 in PCI configuration space returns the Device ID and the Vendor ID. If this bit is set to 1, reading subaddress 0x00 in PCI configuration space returns the Subsystem ID and the Subsystem Vendor ID.

bit 28: PCI Read No Flush Mode. A value of 1 submits a request to not flush the Read FIFO if a PCI Read cycle completes (Read Ahead mode). A value of 0 submits a request to flush the Read FIFO if a PCI Read cycle completes.
BLN 99-13: this bit must be set to 0.

bit 27: Gate Local Bus Latency Timer with BREQ. If set to 0, the PCI 9080 gives up the Local Bus during Direct Slave or DMA transfer after the current cycle. If set to 1, the PCI 9080 gives up the Local Bus only if BREQ is sampled and the Local Bus Latency Timer is enabled and expired during a Direct Slave or DMA transfer.
BLN 99-13: this bit must be set to 0.

bit 26: PCI Read with Write Flush Mode. A value of 1 submits a request to flush a pending Read cycle if a Write cycle is detected. A value of 0 submits a request to not effect pending Reads when a Write cycle occurs (PCI Specification v2.1 compatible).
BLN 99-13: this bit must be set to 0.

bit 25: PCI Read No Write Mode. A value of 1 forces Retry on Writes if read is pending. A value of 0 allows Writes to occur when Read is pending.
BLN 99-13: this bit must be set to 1.

bit 24: PCI Specification v2.1 Mode. When set to 1, the PCI 9080 operates in Delayed Transaction mode for Direct Slave Reads. The PCI 9080 issues a Retry and prefetches read data.
BLN 99-13: this bit must be set to 1.

bit 23: PCI Request Mode. A value of 1 causes the PCI 9080 to de-assert REQ when it asserts FRAME during a Master cycle. A value of 0 causes the PCI 9080 to leave REQ asserted for the entire Bus Master cycle.
BLN 99-13: this bit must be set to 0.

bit 22: Direct Slave LLOCK# Enable. A value of 1 enables PCI Direct Slave locked sequences. A value of 0 disables PCI Direct Slave locked sequences.
BLN 99-13: this bit must be set to 0.

bit 21: Local Bus Direct Slave Give-up Bus Mode. When set to 1, the PCI 9080 de-asserts HOLD and releases the Local Bus when the Direct Slave Write FIFO becomes empty during a Direct Slave Write or when the Direct Slave Read FIFO becomes full during a Direct Slave Read.
BLN 99-13: this bit must be set to 1.

bits 20..19: DMA Channel Priority. The coding of these bits is as follows:

bit 20	bit 19	meaning
0	0	rotational priority scheme
0	1	DMA Channel 0 has priority
1	0	DMA Channel 1 has priority
1	1	reserved

BLN 99-13: as only DMA channel 0 is used, these bits must be set to 01 (DMA Channel 0 has priority)

bit 18: Local Bus BREQ Enable. A value of 1 enables Local Bus BREQ input. When BREQ input is active, the PCI 9080 de-asserts HOLD and releases the Local bus.
BLN 99-13: this bit must be set to 0.

bit 17: Local Bus Pause Timer Enable. A value of 1 enables the Pause Timer, A value of 0 disables the Pause Timer.
BLN 99-13: this bit must be set to 0.

bit 16: Local Bus Latency Timer Enable. A value of 1 enables the Latency Timer, A value of 0 disables the Latency Timer.
BLN 99-13: this bit must be set to 0.

bits 15..8: Local Bus Pause Timer. The number of Local Bus clock cycles before reasserting HOLD after releasing the Local Bus. Only applicable to DMA operation.
BLN 99-13: these bits must be set to 0x00.

bits 7..0: Local Bus Latency Timer. The number of Local Bus clock cycles before de-asserting HOLD and releasing the Local Bus. Also used with bit 27 to delay BREQ input to give up the Local Bus only when this timer expires.
BLN 99-13: these bits must be set to 0x00.

5.1.4 Big/Little Endian Descriptor Register

This 32-bit read/write register at subaddress 0x0c controls Big/Little Endian ordering. The TUeDACS system has a native Little Endian ordering.

This register has the following bits:

bits 31..8: reserved, always read as zero

bit 7: DMA Channel 0 Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering for DMA Channel 0 accesses to the Local Address Space. A value of 0 specifies Little Endian Ordering.
BLN 99-13: this bit must be set to 0 (Little Endian ordering)

bit 6: DMA Channel 1 Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering for DMA Channel 1 accesses to the Local Address Space. A value of 0 specifies Little Endian Ordering.
BLN 99-13: this bit must be set to 0 (DMA channel 1 is not used)

bit 5: Direct Slave Address Space 1 Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering for Direct Slave accesses to the Local Address Space 1. A value of 0 specifies Little Endian ordering.
BLN 99-13: this bit must be set to 0 (Local Address Space 1 is not used)

bit 4: Big Endian Byte Lane Mode. A value of 1 specifies that in Big Endian mode byte lanes [31:16] for 16-bit Local Bus and byte lanes [31:24] for 8-bit Local bus are used. A value of 0 specifies that in Big Endian mode byte lanes [15:0] for 16-bit Local Bus and byte lanes [7:0] for 8-bit Local bus are used.
BLN 99-13: this bit must be set to 0 (Local Address Space 1 is not used)

bit 3: Direct Slave Address Expansion ROM 0 Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering for Direct Slave accesses to the Expansion ROM. A value of 0 specifies Little Endian ordering.
BLN 99-13: this bit must be set to 0 (Expansion ROM is not used)

bit 2: Direct Slave Address Space 0 Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering for Direct Slave accesses to the Local Address Space 0 (registers in the Serial Highway Control section, see section 6). A value of 0 specifies Little Endian ordering.
BLN 99-13: this bit must be set to 0 (Little Endian ordering)

bit 1: Direct Master Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering for Direct Master accesses. A value of 0 specifies Little Endian ordering. Big Endian mode can be specified for Direct Master accesses by asserting the BIGEND# input pin during the address phase of the access.
BLN 99-13: this bit must be set to 0

bit 0: Configuration Register Big Endian Mode. A value of 1 specifies the use of Big Endian data ordering Local accesses to the Configuration registers. A value of 0 specifies Little Endian ordering. Big Endian mode can be specified for Configuration accesses by asserting the BIGEND# input pin during the address phase of the access.
BLN 99-13: this bit must be set to 0

5.1.5 Local Bus Region Descriptors (Space 0 and Expansion ROM) for PCI-to-Local Accesses

This register is loaded from EEPROM, if a programmed EEPROM is present. This 32-bit read/write register at subaddress 0x18 has the following bits:

bits 31..28: PCI Target Retry Delay Clocks. Contains the value (multiplied by 8) of the number of PCI clocks after receiving PCI-to-Local Read or Write accesses and not successfully completing a transfer Only pertains to Direct Slave Writes when bit 27 is set to 1.
BLN 99-13: these bits must be set to 0x4 (= 32 clocks)

bit 27: Direct Slave PCI Write Mode. A value of 0 indicates the PCI 9080 should disconnect when the Direct Slave Write FIFO is full. A value of 1 indicates the PCI 9080 should de-assert TRDY# when the Write FIFO is full.
BLN 99-13: this bit must be set to 0.

bit 26: Expansion ROM Space Burst Enable. A value of 1 enables bursting. A value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.
BLN 99-13: this bit must be set to 0

bit 25: Extra Long Load from Serial EEPROM. A value of 1 loads Subsystem ID and Local Address Space 1 registers. A value of 0 indicates not to load them.
BLN 99-13: this bit must be set to 0 (no Extra Long Load as Local Address Space 1 is not used)

bit 24: Memory Space 0 (= Local Address Space 0) Burst Enable. A value of 1 enables bursting. A value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.
BLN 99-13: this bit must be set to 0 (disable bursting)

bit 23: Expansion ROM Space BTERM Input Enable. A value of 1 enables the BTERM# input. A value of 0 disables the BTERM# input. If set to 0, the PCI 9080 bursts four lwords maximum at a time.
BLN 99-13: this bit must be set to 0 (Expansion ROM not used)

bit 22: Expansion ROM Space Ready Input Enable. A value of 1 enables Ready input. A value of 0 disables Ready input.
BLN 99-13: this bit must be set to 0 (Expansion ROM not used)

bits 21..18: Expansion ROM Space Internal Wait States (data-to-data, 0-15 wait states).
BLN 99-13: these bits must be set to 0x0 (Expansion ROM not used)

bits 17..16: Expansion ROM Space Local bus Width. The coding of these bits is as follows:

bit 17	bit 16	meaning
0	0	bus width 8 bits
0	1	bus width 16 bits
1	0	bus width 32 bits
1	1	bus width 32 bits

BLN 99-13: these bits must be set to 11 (value after reset, Expansion ROM not used)

bit 15: reserved, always read as zero

bits 14..11: Prefetch Counter. Number of Lwords to prefetch during Memory Read cycles (0-15). Count of zero selects prefetch of 16 Lwords.
BLN 99-13: these bits must be set to 0x0 (prefetch 16 Lwords)

bit 10: Read Prefetch Count Enable. When set to 1 and memory prefetching is enabled, the PCI 9080 prefetches up to the number of Lwords specified by Prefetch Counter. When set to 0, the PCI 9080 ignores the count an continues prefetching until terminated by the PCI bus.
BLN 99-13: this bit must be set to 0 (ignore Prefetch Counter)

bit 9: Expansion ROM Space Prefetch Disable. A value of 0 enables Read prefetching. A value of 1 disables prefetching. If prefetching is disabled, the PCI 9080 disconnects after each memory read.
BLN 99-13: this bit must be set to 0

bit 8: Memory Space 0 Prefetch Disable. If mapped into memory space, a value of 0 enables Read prefetching. A value of 1 disables prefetching. If prefetching is disabled, the PCI 9080 disconnects after each memory read.
BLN 99-13: this bit must be set to 0

bit 7: Memory Space 0 BTERM# Input Enable. A value of 1 enables BTERM# input. A value of 0 disables BTERM# input. If set to 0, the PCI 9080 bursts 4 Lword maximum at a time.
BLN 99-13: this bit must be set to 0 (disables BTERM# input)

bit 6: Memory Space 0 Ready Input Enable. A value of 1 enables Ready input. A value of 0 disables Ready input.
BLN 99-13: this bit must be set to 1 (enables Ready input)

bits 5..2: Memory Space 0 Internal Wait States (data-to-data; 0-15 wait states).
BLN 99-13: these bits must be set to 0x0 (0 wait states)

bits 1..0: Memory Space 0 Local Bus Width. The coding of these bits is as follows:

bit 1	bit 0	meaning
0	0	bus width 8 bits
0	1	bus width 16 bits
1	0	bus width 32 bits
1	1	bus width 32 bits

BLN 99-13: these bits must be set to 11 (bus width 32 bits)

5.2 Runtime Registers

The programming model of the Runtime Registers is given in figure 5.3.

Register		Offset
MAILBOX REGISTER 0		0x40
MAILBOX REGISTER 1		0x44
MAILBOX REGISTER 2		0x48
MAILBOX REGISTER 3		0x4C
MAILBOX REGISTER 4		0x50
MAILBOX REGISTER 5		0x54
MAILBOX REGISTER 6		0x58
MAILBOX REGISTER 7		0x5C
PCI-TO-LOCAL DOORBELL REGISTER		0x60
LOCAL-TO-PCI DOORBELL REGISTER		0x64
INTERRUPT CONTROL / STATUS REGISTER		0x68
SERIAL EEPROM CONTROL, PCI COMMAND CODE, USER I/O CONTROL, INIT CONTROL REGISTER		0x6C
DEVICE ID	VENDOR ID	0x70
UNUSED	REVISION ID	0x74
MAILBOX REGISTER 0		0x78
MAILBOX REGISTER		0x7C

Figure 5.3 Runtime Registers programming model

The following Runtime Registers are not used on the PCI/Serial Highway Controller:

	subaddress	register
❑	0x40..0x5c	Mailbox Register 0..7
❑	0x60	PCI-to-Local Doorbell Register
❑	0x64	Local-to-PCI Doorbell Register
❑	0x78	Mailbox Register 0
❑	0x7c	Mailbox Register

5.2.1 Interrupt Control / Status Register

This 32-bit read/write register at subaddress 0x68 has the following bits. A read-only bit is indicated with RO, writing a read-only bit has no effect.

bit 31 (RO): A value of 1 indicates PCI wrote data to MailBox #3. Enabled only if MBOXINTENB is enabled (bit 3 is set to 1).
BLN 99-13: this bit must always read as 0

bit 30 (RO): A value of 1 indicates PCI wrote data to MailBox #2. Enabled only if MBOXINTENB is enabled (bit 3 is set to 1).
BLN 99-13: this bit must always read as 0

bit 29 (RO): A value of 1 indicates PCI wrote data to MailBox #1. Enabled only if MBOXINTENB is enabled (bit 3 is set to 1).
BLN 99-13: this bit must always read as 0

bit 28 (RO): A value of 1 indicates PCI wrote data to MailBox #0. Enabled only if MBOXINTENB is enabled (bit 3 is set to 1).
BLN 99-13: this bit must always read as 0

bit 27 (RO): A value of 0 indicates Target Abort was generated by the PCI 9080 after 256 consecutive Master retries to Target (not valid until abort occurs).

bit 26 (RO): A value of 0 indicates DMA Channel 1 was Bus Master during a Master or Target abort (not valid until abort occurs).

bit 25 (RO): A value of 0 indicates DMA Channel 0 was Bus Master during a Master or Target abort (not valid until abort occurs).

bit 24 (RO): A value of 0 indicates Direct Master was Bus Master during a Master or Target abort (not valid until abort occurs).

bit 23 (RO): A value of 1 indicates BIST (Built-In Self-Test) interrupt is active. Writing a 1 to bit 6 of the PCI Configuration BIST Register generates BIST interrupt. Clearing bit 6 clears the interrupt.
BLN 99-13: this bit must always read as 0

bit 22 (RO): A value of 1 indicates DMA Channel 1 interrupt is active.
BLN 99-13: this bit must always read as 0

bit 21 (RO): A value of 1 indicates DMA Channel 0 interrupt is active.

bit 20 (RO): A value of 1 indicates local doorbell interrupt is active.
BLN 99-13: this bit must always read as 0

bit 19 (R/W): Local DMA Channel 1 Interrupt Enable. A value of 1 enables DMA Channel 1 interrupts. Used in conjunction with Local Interrupt Enable (bit 11). Clearing DMA status bits also clears interrupt.
BLN 99-13: this bit must bet set to 0 (disable Local DMA Channel 1 Interrupt)

bit 18 (R/W): Local DMA Channel 0 Interrupt Enable. A value of 1 enables DMA Channel 0 interrupts. Used in conjunction with Local Interrupt Enable (bit 11). Clearing DMA status bits also clears interrupt.

bit 17 (R/W): Local Doorbell Interrupt Enable. A value of 1 enables doorbell interrupts. Used in conjunction with Local Interrupt Enable (bit 11). Clearing local doorbell interrupt bits that caused interrupt also clears interrupt.
BLN 99-13: this bit must bet set to 0 (disable Local DMA Channel 1 Interrupt)

bit 16 (R/W): Local Interrupt Output Enable. A value of 1 enables Local interrupt output.
BLN 99-13: this bit must bet set to 0.

bit 15 (RO): A value of 1 indicates Local interrupt is active, i.e. the LINTi# input pin is in the asserted state.

bit 14 (RO): A value of 1 indicates PCI abort interrupt is active.

bit 13 (RO): A value of 1 indicates PCI doorbell interrupt is active.
BLN 99-13: this bit must always read as 0

bit 12 (R/W): Retry Abort Enable. A value of 1 enables the PCI 9080 to treat 256 Master consecutive retries to a Target as a Target Abort. A value of 0 enables the PCI 9080 to attempt Master Retries indefinitely. *For diagnostic purposes only.*
BLN 99-13: this bit must be set to 0

bit 11 (R/W): PCI Local Interrupt Enable. A value of 1 enables the Local interrupt input to generate a PCI interrupt. Used in conjunction with the PCI Interrupt Enable bit (bit 8). Clearing the Local Bus cause of interrupt also clears interrupt.

bit 10 (R/W): PCI Abort Interrupt Enable. A value of 1 enables Master abort of Master detect of Target abort to generate PCI interrupt. Used in conjunction with PCI Interrupt Enable (bit 8). Clearing abort status bits also clears PCI interrupt.
BLN 99-13: this bit must be set to 0

bit 9 (R/W): PCI Doorbell Interrupt Enable. A value of 1 enables doorbell interrupts. Used in conjunction with PCI Interrupt Enable (bit 8). Clearing doorbell interrupt bits that caused interrupt also clears interrupt.
BLN 99-13: this bit must be set to 0

bit 8 (R/W): PCI Interrupt Enable. A value of 1 enables PCI interrupts, a value of 0 disables PCI interrupts.

bit 7..4 (RO): reserved
BLN 99-13: these bits must always read as 0

bit 3 (R/W): Mailbox Interrupt Enable. A value of 1 enables a local interrupt to be generated when PCI bus writes to Mailbox Registers 0 through 3. To clear a Local interrupt, the Local Master must read the Mailbox. Used in conjunction with Local Interrupt Enable (bit 11).
BLN 99-13: this bit must be set to 0

bit 2 (R/W): Generate PCI Bus SERR#. When set to 0, writing 1 generates PCI Bus SERR#.
BLN 99-13: this bit must be set to 0

bit 1 (R/W): Enable Local Bus LSERR# when PCI parity error occurs during a PCI 9080 Master Transfer or a PCI 9080 slave access or an Outbound Free List FIFO Overflow Init.
BLN 99-13: this bit must be set to 0

bit 0 (R/W): Enable Local Bus LSERR#. A value of 1 enables the PCI 9080 to assert LSERR# interrupt output when PCI Bus Target Abort or Master Abort Status bit is set in the the PCI Configuration Status Register.
BLN 99-13: this bit must be set to 0

5.2.2 Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register

bit 31 (R/W): Local Init Status. A value of 1 indicates Local Init is done. Responses to PCI accesses are retries until this bit is set. While input pin NB# is asserted (low) this bit is forced to 1.
BLN 99-13: this bit must always read as 0

bit 30 (R/W): PCI Adapter Software Reset. A value of 1 holds Local Bus logic in the PCI 9080 reset and LRESETo# asserted. Setting this bit resets the internal EPLD logic of the Serial Highway Controller section, but does not clear the EPLD *contents.* The contents of PCI Configuration Registers and Shared Runtime Registers are *not* reset. Software Reset can only be cleared from the PCI bus; Local Bus remains reset until this bit is cleared.

bit 29 (R/W): Reload Configuration Registers. When set to 0, writing 1 causes the PCI 9080 to reload Local Configuration Register from the serial EEPROM.

bit 28 (RO): Serial EEPROM Present. A value of 1 indicates that a serial EEPROM is present.
BLN 99-13: this bit must always read as 1

bit 27 (RO): Read Serial EEPROM Data. For Reads, this input bit is the output of the serial EEPROM. Clocked out of serial EEPROM by Serial EEPROM Clock (bit 24).

bit 26 (R/W): Write Bit to serial EEPROM. For Writes, this output bit is the input to the serial EEPROM. Clocked into serial EEPROM by Serial EEPROM Clock (bit 24).

bit 25 (R/W): Serial EEPROM Chip Select. For Local or PCI Bus Reads or Writes to serial EEPROM, setting this bit to 1 provides serial EEPROM chip select.

bit 24 (R/W): Serial EEPROM Clock for Local or PCI Bus Reads or Writes to serial EEPROM. Toggling this bit generates serial EEPROM clock. Refer to manufacturer’s data sheet for particular serial EEPROM being used.

bit 23..18: RO, reserved. These bits always read as 0.

bit 17 (RO): General Purpose Input. A value of 1 indicates USERI input pin is high. A value of 0 indicates USERI input pin is low.
BLN 99-13: this bit must always read as 0.

bit 16 (R/W): General Purpose Output. A value of 1 causes USERO output to go high. A value of 0 causes USERO output to go low.
BLN 99-13: this bit must be set to 0.

bit 15..12 (R/W):
PCI Memory Write Command Code for Direct Master. Sent out during Direct Master Write cycles.
BLN 99-13: these bits must be set to 0x7 (= 0111)

bit 11..8 (R/W):
PCI Memory Read Command Code for Direct Master. Sent out during Direct Master Read cycles.
BLN 99-13: these bits must be set to 0x6 (= 0110)

bit 7..4 (R/W): PCI Write Command Code for DMA. Sent out during DMA Write cycles.
BLN 99-13: these bits must be set to 0x7 (= 0111)

bit 3..0 (R/W): PCI Read Command Code for DMA. Sent out during DMA Read cycles.
BLN 99-13: these bits must be set to 0x6 (= 0110)

5.2.3 Vendor ID

This 16-bit read-only register at subaddress 0x70 identifies the device manufacturer. It is hardcoded to the PCI SIG issued vendor ID of PLX (0x10b5).

5.2.4 Device ID

This 16-bit read-only register at subaddress 0x72 identifies a particular device. It is hardcoded to the PLX part number for PCI interface chip 9080 (0x9080).

5.2.5 Revision ID

This 16-bit read-only register at subaddress 0x74 identifies the current silicon revision of the PCI 9080 interface chip. Bits 7..0 hold the revision level, bits 15..8 always read as zero.

5.3 DMA Registers

The programming model of the DMA Registers is given in figure 5.4.

DMA CHANNEL 0 MODE REGISTER			0x80
DMA CHANNEL 0 PCI ADDRESS REGISTER			0x84
DMA CHANNEL 0 LOCAL ADDRESS REGISTER			0x88
DMA CHANNEL 0 TRANSFER BYTE COUNT REGISTER			0x8C
DMA CHANNEL 0 DESCRIPTOR POINTER REGISTER			0x90
DMA CHANNEL 1 MODE REGISTER			0x94
DMA CHANNEL 1 PCI ADDRESS REGISTER			0x98
DMA CHANNEL 1 LOCAL ADDRESS REGISTER			0x9C
DMA CHANNEL 1 TRANSFER BYTE COUNT REGISTER			0xA0
DMA CHANNEL 1 DESCRIPTOR POINTER REGISTER			0xA4
RESERVED	DMA CHANNEL 1 COMMAND/STATUS REGISTER	DMA CHANNEL 0 COMMAND/STATUS REGISTER	0xA8
MODE/ARBITRATION REGISTER			0xAC
DMA THRESHOLD REGISTER			0xB0

Figure 5.4 DMA Registers programming model

The following DMA Registers are not used on the PCI/Serial Highway Controller:

subaddress	register
❑ 0x94	DMA Channel 1 Mode Register
❑ 0x98	DMA Channel 1 PCI Address Register
❑ 0x9c	DMA Channel 1 Local Address Register
❑ 0xa0	DMA Channel 1 Transfer Byte Count Register
❑ 0xa4	DMA Channel 1 Descriptor Pointer Register
❑ 0xa9	DMA Channel 1 Command/Status Register

5.3.1 DMA Channel 0 Mode Register

This read/write register at subaddress 0x80 has the following bits (all bits are read/write bits):

bits 31..18: RO, reserved. These bits always read as 0.

bit 17: DMA Channel 0 Interrupt Select. A value of 1 routes DMA Channel 0 interrupt to the PCI interrupt. A value of 0 routes DMA Channel 0 interrupt to the Local Bus interrupt.
BLN 99-13: this bit must be set to 1 (PCI interrupt)

bit 16: DMA Clear Count Mode. When set to 1, if it is in Local memory, byte count in each chaining descriptor is cleared when corresponding DMA transfer completes. If the chaining descriptor is in PCI memory, the count is not cleared.
BLN 99-13: the chaining descriptor is in PCI memory. This bit must be set to 0.

bit 15: DMA Stop Data Transfer Mode. A value of 0 sends BLAST to terminate DMA transfer. A value of 1 indicates EOT asserted or DREQ[1:0]# deasserted during Demand mode DMA terminates a DMA transfer.
BLN 99-13: ?

bit 14: DMA EOT (End Of Transfer) Enable. A value of 1 enables EOT[1:0]# input pin. A value of 0 disables EOT[1:0]# input pin.
BLN 99-13: this bit is set if a bus error occurs during a DMA transfer.

bit 13: Write and Invalidate Mode for DMA transfers. When set to 1, the PCI 9080 performs Write and Invalidate cycles to the PCI Bus. The PCI 9080 supports Write and Invalidate sizes of 8 or 16 Lwords. The size is specified in the PCI Cache Line Size Register. If size other than 8 or 16 is specified the PCI 9080 performs Write transfers rather than Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries.
BLN 99-13: this bit must be set to 0.

bit 12: Demand Mode. A value of 1 causes the DMA controller to operate in Demand mode. In Demand mode, the DMA controller transfers data when its DREQ[1:0]# input is asserted. Asserts DACK[1:0]# to indicate current Local Bus transfer is in response to DREQ[1:0]# input. DMA controller transfers Lwords (32 bit) of data. May result in multiple transfers for 8- or 16-bit bus.
BLN 99-13: this bit must be set to 1 (Demand mode)

bit 11: Local Addressing Mode. A value of 1 indicates Local Address bits 31..2 to be held constant. A value of 0 indicates Local Address is incremented.
BLN 99-13: this bit must be set to 1 (constant Local Address address)

bit 10: Done Interrupt Enable. A value of 1 enables interrupt when done. A value of 0 disables interrupt when done. If DMA Clear Count mode is enabled, interrupt does not occur until byte count is cleared.

bit 9: Chaining. A value of 1 indicates Chaining mode is enabled. For Chaining mode, DMA source address, destination address and byte count are loaded from memory in PCI or Local Address Spaces. A value of 0 indicates Non-Chaining mode is enabled.

bit 8: Local Burst Enable. A value of 1 enables local bursting. A value of 0 disables local bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.
BLN 99-13: this bit must be set to 0 (disable local bursting)

bit 7: BTERM# Input Enable. A value of 1 enables BTERM# input. A value of 0 disables BTERM# input. If set to 0, the PCI 9080 bursts 4 Lwords maximum at a time.
BLN 99-13: this bit must be set to 0 (disable BTERM# input)

bit 6: Ready Input Enable. A value of 1 enables the Ready input. A value of 0 disables the Ready input.
BLN 99-13: this bit must be set to 1 (enable Ready input)

bits 5..2: Internal Wait States (data to data).
BLN 99-13: these bits must be set to 0x0

bits 1..0: Local Bus Width. The coding of these bits is as follows:

bit 1	bit 0	meaning
0	0	bus width 8 bits
0	1	bus width 16 bits
1	0	bus width 32 bits
1	1	bus width 32 bits

BLN 99-13: these bits must be set to 10 or 11 (bus width 32 bits)

5.3.2 DMA Channel 0 PCI Address Register

This 32-bit read/write register at subaddress 0x84 indicates from where in PCI memory space the DMA transfers (reads or writes) start.

5.3.3 DMA Channel 0 Local Address Register

This 32-bit read/write register at subaddress 0x88 indicates from where in Local memory space the DMA transfers (reads or writes) start. This register must be initialized with the PCI memory address of the PhyBUS Longword Data Register at subaddress 0x10 or the PhyBUS Word Data Register at subaddress 0x04 in the Serial Highway Control section, see section 6. The base address of the Serial Highway Control section is given by the contents of PCI Base Address Register 2 (PCIBAR2) in the PCI configuration space.

5.3.4 DMA Channel 0 Transfer Byte Count Register

This 32-bit read/write register at subaddress 0x8c indicates the number of bytes to transfer during DMA operation. Bits 22..0 of this register are used, allowing a maximum byte count of 2^{23} (= 4 Mbyte). Bits 31..23 are not used and always read as zero.

5.3.5 DMA Channel 0 Descriptor Pointer Register

This 32-bit read/write register at subaddress 0x90 holds the (first) descriptor for a DMA transfer.

bits 31..4: Next Descriptor Address. These bits hold the address of the next descriptor (quad word aligned, address bits 3..0 = 0x0).

bit 3: Direction of Transfer. A value of 1 indicates DMA transfers from the local bus (TUeDACS bus) to the PCI bus. A value of 0 indicates DMA transfers from the PCI bus to the local bus (TUeDACS bus).

bit 2: Interrupt after Terminal Count. A value of 1 causes an interrupt to be generated after the terminal count for the current descriptor is reached. A value of 0 disables interrupt generation for the current descriptor.

bit 1: End of Chain. A value of 1 indicates that the current descriptor is the end of the chain (no more descriptors). A value of 0 indicates that the current descriptor is *not* the end of the chain; the address of the next descriptor is given by the Next Descriptor Address (bits 31..4).

bit 0: Descriptor Location. A value of 1 indicates the next descriptor is located in PCI Address Space. A value of 0 indicates the next descriptor is located in Local Address Space.
BLN 99-13: this bit must be set to 1 (descriptors always located in PCI Address Space).

5.3.6 DMA Channel 0 Command/Status Register

This 8-bit read/write register at subaddress 0xa8 controls DMA operation of DMA Channel 0.

bits 7..5: reserved, always read as zero.

bit 4: Channel 0 Done. A value of 1 indicates the channel's transfer is complete. A value of 0 indicates the channel's transfer is not complete.

bit 3: Clear Interrupt. Writing a 1 to this write-only bit clears DMA channel 0 interrupts.

bit 2: Channel 0 Abort. Writing a 1 to this write-only bit causes the channel to abort the current transfer. The Channel Enable bit (bit 0) must be cleared. The Channel Complete bit is set when the abort is complete.

bit 1: Channel 0 Start. Writing a 1 to this write-only bit causes the channel to start transferring data if the channel is enabled.

bit 0: Channel 0 Enable. A value of 1 enables the channel to transfer data. A value of 0 disables the channel from starting a DMA transfer, and, if in process of transferring data, suspends the transfer (pause).

5.3.7 DMA Mode/Arbitration Register

See the description of the Mode/Arbitration Register at subaddress 0x04.

5.3.8 DMA Threshold Register

This 32-bit register at subaddress 0xb0 sets the FIFO thresholds for local bus / PCI bus requests during DMA transfers.

BLN 99-13: as DMA Channel 1 is not used, bits 31..16 are not used anf can be set to 0x0000.

bits 31..28: DMA Channel 1 PCI-to-Local Almost Empty (C1PLAE). Number of empty entries (minus one) in the FIFO before requesting PCI Bus for reads.

bits 27..24: DMA Channel 1 Local-to-PCI Almost Full (C1LPAF). Number of full entries (minus one) in the FIFO before requesting PCI Bus for writes.

bits 23..20: DMA Channel 1 Local-to-PCI Almost Empty (C1LPAE). Number of empty entries (minus one) in the FIFO before requesting Local Bus for reads.
(C1PLAF) + (C1PLAE) should be ≤ FIFO depth of 16.

bits 19..16: DMA Channel 1 PCI-to-Local Almost Full (C1PLAF). Number of full entries (minus one) in the FIFO before requesting Local Bus for writes.
(C1PLAF + 1) + (C1PLAE + 1) should be ≤ FIFO depth of 16.

bits 15..12: DMA Channel 0 PCI-to-Local Almost Empty (C0PLAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting PCI Bus for reads.

bits 11..8: DMA Channel 0 Local-to-PCI Almost Full (C0LPAF). Number of full entries (divided by two, minus one) in the FIFO before requesting PCI Bus for writes.

bits 7..4: DMA Channel 0 Local-to-PCI Almost Empty (C0LPAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting Local Bus for reads.
(C0LPAF + 1) + (C0LPAE + 1) should be ≤ FIFO depth of 32.

bits 3..0: DMA Channel 0 PCI-to-Local Almost Full (C0PLAF). Number of full entries (divided by two, minus one) in the FIFO before requesting Local Bus for writes.
(C0PLAF + 1) + (C0PLAE + 1) should be ≤ FIFO depth of 32.

6. Programming model of the Serial Highway control section

The programming model of the Serial Highway control section is given in figure 6.1. This section controls TUeDACS bus accesses to and from a TUeDACS system crate or a TUeDACS interface module.

All subaddresses in the programming model of the Serial Highway control section are relative to the base address contained in PCI Base Address Register 2 for Local Address Space 0 (PCIBAR2). PCIBAR2 is located in the PCI configuration space, see section 4. The PCIBAR2 register holds the physical memory start address in system memory space of the Serial Highway control registers.

Subaddresses in the Serial Highway control section are only accessible if the MS-bit (Memory Space) in the Command Register in the PCI configuration space is set. See section 4.3 and figure 4.2. If the MS bit is cleared, read/write accesses from or to the Serial Highway control section are disabled.

CONTROL AND STATUS REGISTER	0x00
PHYBUS (DMA) ADDRESS REGISTER	0x04
PHYBUS WORD DATA REGISTER	0x08
INTERRUPT ENQUIRY REGISTER	0x0C
PHYBUS LONG WORD DATA REGISTER	0x10
MAINTENANCE CSR	0x14
MAINTENANCE WORD DATA REGISTER	0x18
MAINTENANCE LONG WORD DATA REGISTER	0x1C
PROTOCOL ERROR REGISTER SLAVE	0x20
PROTOCOL ERROR REGISTER MASTER	0x24
INTERRUPT CONTROL AND STATUS REGISTER	0x28
BUS ERROR ADDRESS REGISTER	0x2C
SWAP SELECT REGISTER	0x30
EPLD CONFIGURATION REGISTER	0x34
	0x38
	0x3C

Figure 6.1 Programming model of the Serial Highway control section

6.1 Control and Status Register

This 16-bit read/write register at subaddress 0x00 controls the general operation of the Serial Highway.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PE	PEM	PES	X	X	X	X	X	X	IE	RST	X	PER	BT	MNT	ISP	0x00

Figure 6.2 Control and Status Register

bit	mnemonic	R/W	description
15	PE	RO	Protocol Error
14	PEM	RO	Protocol Error Master
13	PES	RO	Protocol Error Slave
12..7	-	-	not used, reads as zero
6	IE	R/W	Interrupt Enable
5	RST	WO	ReSeT
4	-	-	not used, reads as zero
3	PER	WO	Protocol Error Reset
2	BT	R/W	Block Transfer
1	MNT	R/W	MaiNTenance operation select
0	ISP	WO	Init Slave PhyBUS

PE (bit 15): Protocol Error. This read-only bit indicates that a protocol error has occurred; this bit is the logical OR function of the PEM bit and the PES bit. A protocol error (either at the master side and/or the slave side) is specified by the contents of the Protocol Error Registers at subaddresses 0x20 (slave) and 0x24 (master).

The PE bit is cleared when setting the RST bit, when setting the PER bit, or when issuing a software TUeDACS bus initialisation command.

PEM (bit 14): Protocol Error Master. This read-only bit indicates that a protocol error has occurred at the master side of the Serial Highway. The protocol error is specified by the contents of the Protocol Error Register Master at subaddress 0x24.

The PEM bit is cleared when setting the RST bit, when setting the PER bit, or when issuing a software TUeDACS bus initialisation command.

PES (bit 13): Protocol Error Slave. This read-only bit indicates that a protocol error has occurred at the slave side of the Serial Highway. The protocol error is specified by the contents of the Protocol Error Register Slave at subaddress 0x20.

The PES bit is cleared when setting the RST bit, when setting the PER bit, or when issuing a software TUeDACS bus initialisation command.

IE (bit 6): Interrupt Enable. If this bit is set, a PCI interrupt is generated when one or more of the following conditions occur (see also the description of the Interrupt Control and Status Register in section 6.11):

- ❑ a TUeDACS interface generates an interrupt, and the PBIE bit in the Interrupt Control and Status Register at subaddress 0x28 is set,
- ❑ a master or slave protocol error has occured (i.e. the PE bit in the Control and Status register is set), and the PEIE bit in the Interrupt Control and Status Register at subaddress 0x28 is set,
- ❑ a TUeDACS bus read bus error or write bus error has occurred and the BEIE bit in the Interrupt Control and Status Register at subaddress 0x28 is set,
- ❑ a maintenance interrupt is generated by setting the GMI bit in the Interrupt Control and Status Register at subaddress 0x28.

If the IE bit is cleared, no PCI interrupts can be generated. The IE bit acts as a 'master' interrupt enable bit.

The IE bit is cleared when setting the RST bit or when issuing a software TUeDACS bus initialisation command.

RST (bit 5): ReSeT. Setting this bit initialises the Serial Highway control section and resets the corresponding internal logic. The RST bit does NOT reset the TUeDACS bus connected to the PCI/Serial Highway Controller, nor does it reset the EPLD's!
Setting the RST bit is a one-time command. This bit need not be cleared.

PER (bit 3): Protocol Error Reset. Setting this bit clears the PE bit, the PEM bit and the PES bit.
Setting the PER bit is a one-time command. This bit need not be cleared.

BT (bit 2): Block Transfer. Setting this bit selects block transfer for reading data from or writing data to a TUeDACS module or a TUeDACS interface located in a TUeDACS system crate. If block transfer is selected (BT bit is set), *only* the first read or write transfer uses the PhyBUS Address Register at subaddress 0x04 to select a TUeDACS interface (sub)address. All subsequent read and write transfers use this same TUeDACS address, as long as the BT bit is set. This mechanism is used to perform efficient block transfers to or from a TUeDACS interface, and is useful to read from or write to auto-increment registers.

MNT (bit 1): Maintenance operation select. Setting this bit enables the PCI/Serial Highway Controller for maintenance operation. A specific maintenance mode is selected with the MM2, MM1, and MM0 bits in the Maintenance Control and Status Register at subaddress 0x14. See section 7 for a description of the maintenance modes.

ISP (bit 0): Init Slave PhyBUS. Setting this bit generates a global TUeDACS bus initialisation signal in the TUeDACS crate or in the connected TUeDACS/1 interface module. If this initialisation signal is not acknowledged by the TUeDACS crate or by the TUeDACS/1 interface module, the BERI bit in the Interrupt Control and Status Register at subaddress 0x28 is set.
Setting the ISP bit is a one-time command. This bit need not be cleared.

6.2 PhyBUS (DMA) Address Register

This 16-bit write-only register at subaddress 0x04 must be initialized with a TUeDACS interface address. After the address is written to this register, data can be read from or written to the corresponding address by reading or writing the PhyBUS Word Data Register at subaddress 0x08 (16-bit data transfer) or the PhyBUS Long Word Data Register at subaddress 0x10 (32-bit data transfer).

The PhyBUS (DMA) Address Register is write-only, except if maintenance operation in maintenance mode 0 and 2 is selected. In these cases, this register is a read/write register.

X	X	X	X	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	0x04
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.3 PhyBUS Address Register

As TUeDACS bus addresses are in the range 0..4095, only bits 0..11 in this register are used. Bits 12..15 are not used and always read as zero, writing these bits has no effect.

If block transfer is required, application software must use the following sequence:

1. set the BT bit in the Control and Status Register at subaddress 0x00,
2. initialize the PhyBUS Address Register with the required TUeDACS address,
3. execute the required number of read and/or write accesses by reading or writing the PhyBUS Word Data Register (subaddress 0x08) or the PhyBUS Long Word Data Register (subaddress 0x10).

6.3 PhyBUS Word Data Register

This 16-bit read/write register at subaddress 0x08 is used for reading 16-bit data from or writing 16-bit data to the TUeDACS address defined by the contents of the PhyBUS Address Register at subaddress 0x04.

Writing the PhyBUS Word Data Register starts a 16-bit write-transfer from the PCI/Serial Highway Controller to the TUeDACS bus, i.e. data is transferred from the host computer to the TUeDACS bus.

Reading the PhyBUS Word Data Register starts a 16-bit read-transfer from the TUeDACS bus to the PCI/Serial Highway Controller, i.e. data is transferred from the TUeDACS bus to the host computer.

6.4 Interrupt Enquiry Register

This 16-bit read-only register at subaddress 0x0c identifies the TUeDACS interface(s) in the TUeDACS bus or in a TUeDACS/1 interface module that has/have generated an interrupt. Each bit in this register corresponds to a TUeDACS bus data line associated with a specific TUeDACS interface. If a bit in the Interrupt Enquiry Register is set, an interrupt has been generated by a TUeDACS interface of which the corresponding interrupt bit has been selected, and whose interrupt has been enabled. If a bit in the Interrupt Enquiry Register is cleared, the corresponding interface has not generated an interrupt.

NOTE 1: reading the Interrupt Enquiry Register generates an Interrupt Enquiry Cycle on the TUeDACS bus, thereby removing the cause of the interrupt.

NOTE 2: reading the Interrupt Enquiry Register automatically clears this register for the next TUeDACS bus interrupt cycle! In order to handle all interrupts properly, it is necessary to copy the contents of this register into a variable or processor data register.

6.5 PhyBUS Long Word Data Register

This 32-bit read/write register at subaddress 0x10 is used for reading 32-bit data from or writing 32-bit data to the TUeDACS address defined by the contents of the PhyBUS Address Register at subaddress 0x04. Note that the TUeDACS address must be *even* when executing a 32-bit read or write transfer; using an odd TUeDACS address results in a bus error!

Writing the PhyBUS Long Word Data Register starts a 32-bit write-transfer from the PCI/Serial Highway Controller to the TUeDACS bus, i.e. data is transferred from the host computer to the TUeDACS bus.

Reading the PhyBUS Word Data Register starts a 32-bit read-transfer from the TUeDACS bus to the PCI/Serial Highway Controller, i.e. data is transferred from the TUeDACS bus to the host computer.

6.6 Maintenance Control and Status Register

This 16-bit read/write register at subaddress 0x14 is used to test and diagnose the Serial Highway control section in maintenance mode, i.e. the MNT bit in the Control and Status Register at subaddress 0x00 must be set.

X	X	X	X	X	X	X	ITM	INM	X	RST	TPES	TIRQ	MM2	MM1	MM0	0x14
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.4 Maintenance Control and Status Register

bit	mnemonic	R/W	description
15..9	-	-	not used, read as zero
8	ITM	RO	InterrupT enquiry Maintenance
7	INM	RO	INit Maintenance
6	-	-	not used, reads as zero
5	RST	WO	ReSeT Maintenance Control and Status Register
4	TPES	WO	Test Protocol Error Slave (maintenance mode 2)
3	TIRQ	WO	Test Interrupt ReQuest (maintenance mode 2)
2	MM2	R/W	Maintenance Mode select, bit 2
1	MM1	R/W	Maintenance Mode select, bit 1
0	MM0	R/W	Maintenance Mode select, bit 0

ITM (bit 8): InterrupT enquiry Maintenance (maintenance mode 2). This bit is cleared by setting the RST bit in the Maintenance Control and Status Register at subaddress 0x00.

INM (bit 7): INit Maintenance. This bit is cleared by setting the RST bit in the Maintenance Control and Status Register at subaddress 0x00.

RST (bit 5): ReSeT Maintenance Control and Status Register. Setting this write-only bit clears the ITM bit and the INM bit in the Maintenance Control and Status Register at subaddress 0x00.
Setting the RST bit is a one-time command. This bit need not be cleared.

TPES (bit 4): Test Protocol Error Slave (maintenance mode 2). Setting this bit sets the PES bit (and thus the PE bit) in the Control and Status Register at subaddress 0x00, if maintenance mode 2 is selected. See section 7.3.
Setting the TPES bit is a one-time command. This bit need not be cleared.

TIRQ (bit 3): Test Interrupt ReQuest (maintenance mode 2). Setting this bit generates a PhyBUS interrupt if maintenance mode 2 is selected. See section 7.3.
Setting the TIRQ bit is a one-time command. This bit need not be cleared.

MM2..MM0 (bits 2..0): Maintenance Mode select bits 2..0. These bits select a maintenance mode for the Serial Highway control section. Maintenance modes 0..2 are available. Selecting a maintenance mode in the range 3..7 results in undefined operation. See section 7 for a description of the maintenance modes.

6.7 Maintenance Word Data Register

This 16-bit read/write register at subaddress 0x18 is used in maintenance mode 1. See section 7.1 for a description of this maintenance mode.

6.8 Maintenance Long Word Data Register

This 32-bit read/write register at subaddress 0x1c is used in maintenance mode 1. See section 7.1 for a description of this maintenance mode.

6.9 Protocol Error Register Slave

If a protocol error at the slave side (TUeDACS interface in TUeDACS system crate, or a TUeDACS interface module) has occurred during transmission, this 16-bit read-only register at subaddress 0x20 can be used to determine the specific error. A slave protocol error is indicated by the PE and the PES bit in the Control and Status Register at subaddress 0x00.

X	X	X	X	X	X	X	X	X	PES6	PES5	PES4	PES3	PES2	PES1	PES0	0x20
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.5 Protocol Error Register Slave

bit	mnemonic	R/W	description
15..7	-	-	not used, read as zero
6	PES6	RO	Protocol Error Slave, error 6
5	PES5	RO	Protocol Error Slave, error 5
4	PES4	RO	Protocol Error Slave, error 4
3	PES3	RO	Protocol Error Slave, error 3
2	PES2	RO	Protocol Error Slave, error 2
1	PES1	RO	Protocol Error Slave, error 1
0	PES0	RO	Protocol Error Slave, error 0

PES6 (bit 6): Protocol Error Slave 6. This bit is set if the slave has detected an invalid check code when receiving an Interrupt Enquiry message from the master.

PES5 (bit 5): Protocol Error Slave 5. This bit is set if the slave has detected an invalid check code when receiving a TUeDACS initialization message from the master.

PES4 (bit 4): Protocol Error Slave 4. This bit is set if the slave has detected a Read message and a Write message at the same time.

PES3 (bit 3): Protocol Error Slave 3. This bit is set if the slave has detected an invalid number of SYNC-CLOCK pulses during a block read transfer.

PES2 (bit 2): Protocol Error Slave 2. This bit is set if the slave has detected an invalid number of SYNC-CLOCK pulses during a normal (i.e. non-block) read transfer.

PES1 (bit 1): Protocol Error Slave 1. This bit is set if the slave has detected an invalid number of SYNC-CLOCK pulses during a block write transfer.

PES0 (bit 0): Protocol Error Slave 0. This bit is set if the slave has detected an invalid number of SYNC-CLOCK pulses during a normal (i.e. non-block) write transfer.

6.10 Protocol Error Register Master

If a protocol error at the master side (PCI/Serial Highway Controller) has occurred during transmission, this 16-bit read-only register at subaddress 0x24 can be used to determine the specific error. A slave protocol error is indicated by the PE and the PEM bit in the Control and Status Register at subaddress 0x00.

X	X	X	X	X	X	X	X	X	X	PEM5	PEM4	PEM3	PEM2	PEM1	PEM0	0x24
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.6 Protocol Error Register Master

bit	mnemonic	R/W	description
15..4	-	-	not used, read as zero
3	PEM3	RO	Protocol Error Master, error 3
2	PEM2	RO	Protocol Error Master, error 2
1	PEM1	RO	Protocol Error Master, error 1
0	PEM0	RO	Protocol Error Master, error 0

PEM3 (bit 3): Protocol Error Master 3. This bit is set if an error occurs during a read transfer. The number of ACK-CLOCK pulses exceeds 20.

PEM2 (bit 2): Protocol Error Master 2. This bit is set if an error occurs during a write transfer. The number of ACK-CLOCK pulses exceeds 8.

PEM1 (bit 1): Protocol Error Master 1. This bit is set if an invalid check code is detected during a write transfer.

PEM0 (bit 0): Protocol Error Master 0. This bit is set if an invalid check code is detected when receiving an Interrupt Request message from the slave.

6.11 Interrupt Control and Status Register

This 16-bit read/write register at subaddress 0x10 controls the generation of PCI interrupts.

PBI	PEI	BERW	BERR	BERI	BE32	X	X	X	X	X	X	GMI	BEIE	PEIE	PBIE	0x28
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.7 Interrupt Control and Status Register

bit	mnemonic	R/W	description
15	PBI	R/W	PhyBUS Interrupt
14	PEI	R/W	Protocol Error Interrupt
13	BERW	R/W	PhyBUS Bus ERror on Write
12	BERR	R/W	PhyBUS Bus ERror on Read
11	BERI	R/W	PhyBUS Bus ERror on Initialisation
10	BE32	R/W	PhyBUS 32-bits Bus ERror
9..4	-	-	not used, read as zero
3	GMI	WO	Generate Maintenance Interrupt
2	BEIE	R/W	Bus Error Interrupt Enable
1	PEIE	R/W	Protocol Error Interrupt Enable
0	PBIE	R/W	PhyBUS Interrupt Enable

PBI (bit 15): PhyBUS Interrupt. This bit is set if the PCI/Serial Highway Controller receives an interrupt message from the TUeDACS bus, indicating that a TUeDACS interface has generated an interrupt. If the PBIE bit in the Interrupt Control and Status Register AND the IE bit in the Control and Status Register at subaddress 0x00 are set AND the PLX9080 interrupt control bits have been initialized correctly, a PCI interrupt is generated.
The PBI bit must be cleared by writing a 1 to this bit.

PEI (bit 14): Protocol Error Interrupt. This bit is set if a master protocol error or a slave protocol error occurs. In this case, the PE bit and the PES and/or PEM in the Control and Status Register at subaddress 0x00 are also set. If the PEIE bit in the Interrupt Control and Status Register AND the IE bit in the Control and Status Register at subaddress 0x00 are set AND the PLX9080 interrupt control bits have been initialized correctly, a PCI interrupt is generated.
The PEI bit must be cleared by writing a 1 to this bit.

BERW (bit 13): Bus ERror on Write. This bit is set if a bus error occurs when writing to a non-existent or non-accessable TUeDACS bus address. If the bus error occurred when writing to a long-word address, the BE32 bit is also set. The time-out period when writing a TUeDACS bus address is 10 µsec. If the BEIE bit in the Interrupt Control and Status Register AND the IE bit in the Control and Status Register at subaddress 0x00 are set AND the PLX9080 interrupt control bits have been initialized correctly, a PCI interrupt is generated.
The BERW bit must be cleared by writing a 1 to this bit.

BERR (bit 12): Bus ERror on Read. This bit is set if a bus error occurs when reading a non-existent or non-accessable TUeDACS bus address. If the bus error occurred when reading from a long-word address, the BE32 bit is also set. The time-out period when reading a TUeDACS bus address is 10 µsec. If the BEIE bit in the Interrupt Control and Status Register AND the IE bit in the Control and Status Register at subaddress 0x00 are set AND the PLX9080 interrupt control bits have been initialized correctly, a PCI interrupt is generated.
The BERR bit must be cleared by writing a 1 to this bit.

BERI (bit 11): Bus ERror on Initialising TUeDACS bus. This bit is set when a TUeDACS bus initialisation command is not acknowledged by the TUeDACS crate or by a TUeDACS interface module. The initialisation command is generated upon setting the ISP bit in the Control and Status Register at subaddress 0x00.
The BERI bit must be cleared by writing a 1 to this bit.

BE32 (bit 10): PhyBUS 32-bits Bus ERror. This bit is set when a 32-bit read bus error or a 32-bit write bus error has occurred. If the BE32 bit is set, the BERR bit or the BERW bit is also set. The BE32 bit can never be set when reading or writing a TUeDACS 16-bit word address!
The BE32 bit must be cleared by writing a 1 to this bit.

GMI (bit 3): Generate Maintenance Interrupt. Setting this bit immediately generates an interrupt on the PCI bus. Note that the IE bit in the Control and Status Register at subaddress 0x00 need not be set to enable the generation of maintenance interrupts! The GMI bit is used for testing bare PCI interrupt handling. Do not use this bit during normal operation.

BEIE (bit 2): Bus Error Interrupt Enable. Setting this bit enables PCI interrupt generation if a TUeDACS read- or write bus error occurs. See the description of the BERR bit and the BERW bit. Clearing the BEIE bit disables bus error interrupts.

PEIE (bit 1): Protocol Error Interrupt Enable. Setting this bit enables PCI interrupt generation if a master- or slave protocol error occurs. See the decription of the PEI bit. Clearing the PEIE bit disables these interrupts.

PBIE (bit 0): PhyBUS Interrupt Enable. Setting this bit enables PCI interrupt generation if a TUeDACS bus interrupt occurs. See the decription of the PBI bit. Clearing the PBI bit disables these interrupts.

6.12 Bus Error Address Register

This 16-bit read-only register at subaddress 0x2c holds the TUeDACS bus address where the last bus error has occurred (either a read bus error or a write bus error).

X	X	X	X	EA11	EA10	EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0	0x2C
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.8 Bus Error Address Register

6.13 Swap Select Register

This 16-bit read/write register at subaddress 0x30 selects the data swap mode for bytes and/or words for TUeDACS data. The swap mode offers the ability to use the TUeDACS system in both little-endian (e.g. x86 processors) or big-endian (e.g. Motorola M68xxx) hardware environments.

Data swapping only affects data read from or written to the PhyBUS Word Data Register at subaddress 0x08, the PhyBUS Longword Data Register at subaddress 0x10, the PhyBUS Maintenance Word Data Register at subaddress 0x18 and the PhyBUS Maintenance Longword Data Register at subaddress 0x1c.

X	X	X	X	X	X	X	X	X	X	X	X	X	X	SMS1	SMS0	0x30
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.9 Swap Select Register

bit	mnemonic	R/W	description
15..2	-	-	not used, read as zero
1	SMS1	R/W	Swap Mode Select, bit 1
0	SMS0	R/W	Swap Mode Select, bit 0

SMS1..SMS0 (bits 1..0): Swap Mode Select bits 1..0. These bits to select the swap mode for bytes and/or words for TUeDACS data. See table 6.1 for a description of the swap modes.

SMS1	SMS0	swap mode
0	0	normal [0 1 2 3]
0	1	swap bytes in word [1 0 3 2]
1	0	swap words in longword [2 3 1 0]
1	1	swap bytes in word & words in longword [3 2 1 0]

Table 6.1 Swap mode selection

6.14 EPLD Configuration Register

This 16-bit read/write register at subaddress 0x34 is used to load EPLD configuration data. Configuration data can be read from an RBF disk file. After the configuration data has been loaded successfully, the PCI/Serial Highway Controller is available for use.

> **IMPORTANT**:
>
> do not access the registers in the subaddress range 0x00..0x30 of the PCI/Serial Highway Controller *before* the EPLD's have been loaded: this will result in erroneous operation of the PCI/Serial Highway Controller!

X	X	X	X	X	X	X	X	X	X	X	CLR	CLK	DATA	RSD	DONE	0x34
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 6.10 EPLD Configuration Register

bit	mnemonic	R/W	description
15..5	-	-	not used, reads as zero
4	CLR	R/W	CLeaR EPLD's
3	CLK	R/W	CLocK
2	DATA	R/W	DATA
1	RSD	RO	ReSet Done
0	DONE	RO	DONE

CLR (bit 4): CLeaR EPLD's. Setting this read/write bit clears the configuration data of the EPLD's, after which the EPLD's can be (re)loaded. The CLR bit must be cleared to enable EPLD (re)loading.

CLK (bit 3): setting this bit clocks the data contained in the DATA bit (bit 2) in the EPLD Configuration Register, into the EPLD's. Data contained in the DATA bit is part of the EPLD configuration data file.

In order to clock the next data bit, the CLK bit must be cleared first.

DATA (bit 2): DATA. This bit contains a the configuration data bit for the EPLD's. The data from this bit is loaded into the EPLD's upon setting the CLK bit. Data for the DATA bit must be read from an EPLD configuration file (RBF file).

RSD (bit 1): ReSet Done. If this bit is set, the EPLD's are ready to accept (new) configuration data to be loaded using the CLK bit and the DATA bit. If the RSD bit is cleared, the EPLD's are *not* ready to accept configuration data. The RSD bit is cleared when setting the CLR bit, indicating that the EPLD is being reset. The RSD bit is set after the CLR bit is cleared.

DONE (bit 0): DONE. If this bit is set, the EPLD's have been configured successfully (configuration is done). This bit is cleared after power-up or when *clearing* the CLR bit.

7. Description of the maintenance modes

The Serial Highway control section of the PCI/Serial Highway Controller can be tested and diagnosed by using maintenance modes. Maintenance operation is enabled by setting the MNT bit (bit 1) in the Control and Status Register at subaddress 0x00. A specific maintenance mode is selected with the MM2..MM0 bits in the Maintenance Control and Status Register at subaddress 0x14.

7.1 Maintenance mode 0

Maintenance mode 0 is used to execute read/write tests on the following registers:

- ❏ PhyBUS (DMA) Address Register, subaddress 0x04
- ❏ PhyBUS Word Data Register, subaddress 0x08
- ❏ PhyBUS Long Word Data Register, subaddress 0x10

7.2 Maintenance mode 1

Maintenance mode 1 is used to test data and control lines from the master to an (internal) maintenance slave register. An external loopback connector is required for this maintenance mode. Read/write tests can be executed on the following registers:

- ❏ PhyBUS (DMA) Address Register, subaddress 0x04
- ❏ Maintenance Word Data Register, subaddress 0x18
- ❏ Maintenance Long Word Data Register, subaddress 0x1c

The minimum delay time between writing one of these registers and reading the same register to obtain the data previously written, is defined by the Serial Highway protocol, and is approximately 5 μs (depends on the transfer).

7.3 Maintenance mode 2

Maintenance mode 2 is used to test data and control lines from a simulated slave to the master. An external loopback connector is required for this maintenance mode. The following tests can be executed:

- simulate a slave interrupt. This is tested by setting the TIRQ bit in the Maintenance Control and Status Register at subaddress 0x14. If the IE bit in the Control and Status Register at subaddress 0x00 has been set, a TUeDACS interrupt is generated. The delay time between setting the TIRQ bit and the interrupt being generated is defined by the Serial Highway protocol, and is approximately 1 μs.

  The contents of the Interrupt Enquiry Register at subaddress 0x0c is undefined!

- simulate a slave protocol error. This is tested by setting the TPES bit in the Maintenance Control and Status Register at subaddress 0x14. Setting this bit sets the PES and the PE bit in the Control and Status Register at subaddress 0x00. The delay time between setting the TPES bit and the PES and PE bits being set, is defined by the Serial Highway protocol, and is approximately 1 μs.

  Additional testing can be performed by writing data in the range 0..127 to the PhyBUS Word Data Register at subaddress 0x08. When the PES and PE bit are set, the Protocol Error Register Slave at subaddress 0x20 should hold the the data written to the PhyBUS Word Data Register.

Appendix A. Serial EEPROM initialisation data

The serial EEPROM should contain the following values for initialising the PCI 9080 registers:

Serial EEPROM Offset	description	value
0x00	Device ID	0x0002
0x02	Vendor ID	0xfffe
0x04	Class Code	0x0680
0x06	Class Code / Revision	0x0000
0x08	Max_Lat / Min_Gnt	0x0000
0x0a	Interrupt Pin / Interrupt Line Routing	0x0100
0x0c	MSW of Mailbox 0 (User Defined)	0x0000
0x0e	LSW of Mailbox 0 (User Defined)	0x0000
0x10	MSW of Mailbox 1 (User Defined)	0x0000
0x12	MSW of Mailbox 1 (User Defined)	0x0000
0x14	MSW of Range for PCI-to-Local Address Space 0	0xffff
0x16	LSW of Range for PCI-to-Local Address Space 0	0xffc0
0x18	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	0x0000
0x1a	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	0x0001
0x1c	MSW of Local Arbitration Register	0x0328
0x1e	LSW of Local Arbitration Register	0x0000
0x20	MSW of Local Bus Big/Little Endian Descriptor Register	0x0000
0x22	LSW of Local Bus Big/Little Endian Descriptor Register	0x0000
0x24	MSW of Range for PCI-to-Local Expansion ROM	0x0000
0x26	LSW of Range for PCI-to-Local Expansion ROM	0x0000
0x28	MSW of Local Base Address (Remap) for PCI-to-Local ROM	0x0000
0x2a	LSW of Local Base Address (Remap) for PCI-to-Local ROM	0x0000
0x2c	MSW of Bus Region Descriptors for PCI-to-Local Accesses	0x4803
0x2e	LSW of Bus Region Descriptors for PCI-to-Local Accesses	0x0043
0x30	MSW of range for Direct Master to PCI	0x0000
0x32	LSW of range for Direct Master to PCI	0x0000
0x34	MSW of Local Base Address for Direct Master to PCI Memory	0x0000
0x36	LSW of Local Base Address for Direct Master to PCI Memory	0x0000
0x38	MSW of Local Bus Address for Direct Master to PCI IO/CFG	0x0000
0x3a	LSW of Local Bus Address for Direct Master to PCI IO/CFG	0x0000
0x3c	MSW of PCI Base Address (Remap) for Direct Master to PCI	0x0000
0x3e	LSW of PCI Base Address (Remap) for Direct Master to PCI	0x0000

Serial EEPROM Offset	description	value
0x40	MSW of PCI Configuration Address Register for Direct Master to PCI IO/CFG	0x0000
0x42	LSW of PCI Configuration Address Register for Direct Master to PCI IO/CFG	0x0000
0x44	Subsystem ID	0x9913
0x46	Subsystem Vendor ID	0x424c
0x48	MSW of Range PCI-to-Local Address Space 1 (1 MB)	0x0000
0x4a	LSW of Range PCI-to-Local Address Space 1 (1 MB)	0x0000
0x4c	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	0x0000
0x4e	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	0x0000
0x50	MSW of Bus Region Descriptors (Space 1) for PCI-to-local accesses	0x0000
0x52	LSW of Bus Region Descriptors (Space 1) for PCI-to-local accesses	0x0000
0x54	MSW of PCI Base Address for Local Expansion ROM	0x0000
0x56	LSW of PCI Base Address for Local Expansion ROM	0x0000